A CMOS Current-Mode Band-Pass Filter with Small Chip Area

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ABSTRACT

In this paper, we propose a CMOS current-mode band-pass filter with small chip area. Q (quality factor) of the proposed filter can be mostly determined by the ratio of the two MOSFETs' transconductances in a Q-setting part, not by the ratio of the values of two capacitance similar to the conventional band-pass filter. Therefore, the proposed filter does not need large capacitance that occupies large area on an IC chip, being different from the conventional one. The proposed filter needs smaller area than the conventional one under the condition of $Q > 2$. The proposed circuit is simulated by SPICE to confirm its characteristics.

Keywords

CMOS, Analog circuits, Current-mode, filter

1. INTRODUCTION

A band-pass filter is one of important building blocks in analog signal processing used as a channel selection filter in communication devices and so on. In general, filters tend to occupy large area on an IC chip with their capacitors. However, since a manufacturing cost is proportional to the chip area, area efficiency of filters has been demanded.

In the meantime, band-pass filters using parasitic capacitances effectively have been proposed [1]. This type of filters have a merit of high-speed operation and small chip area. However, the passband of this type of filters is commonly limited over 100MHz. Thus, in case that filters with passband in 1-100 MHz is needed, capacitors in parallel with the parasitic capacitance (*Additional Capacitor*) need to be added on the IC chip. Therefore, in general, chip area of the filter with passband in 1-100 MHz tend to have a large chip area. This is a problem to integration.

A band-pass filter we have proposed [2] have the problem with exception. Especially, in case that higher Q value is designed, the problem became notable.

Therefore, a band-pass filter with small chip area is proposed in this paper. This filter uses Q-enhancement technique as a solution of the problem. By using this technique, the proposed filter can be reduce chip area of the filter than the conventional one. The proposed circuit is realized with CMOS technology from the viewpoint of the digital-analog mixed LSI, and with current-mode technique from the viewpoint of the high speed operation and low supply voltage.

2. CONVENTIONAL CIRCUIT

Figure 1 shows a conventional band-pass filter we have proposed in [2], and Eq. (1) shows the transfer function of this circuit. Where g_{mi} is a transconductance of MOSFETs M_{ni} (i=1, 2, 3, 4, 5). $1/g_{mi} << r_{ds}$ (r_{ds} : the drain-source resistance) is assumed. Output resistance of the bias current source I_{BIAS} is ignored.

$$T(s) = \frac{-\dfrac{g_{m2}}{sC_1 + g_{m1}} \dfrac{g_{m3}}{g_{m2}}}{1 + \dfrac{g_{m2}}{sC_1 + g_{m1}} \dfrac{g_{m4}}{sC_2 + g_{m4}} \dfrac{sC_3 + g_{m5}}{sC_3}} \qquad (1)$$

Supposing that $g_{mA}=g_{m1}=g_{m2}=g_{m3}$, $g_{mB}=g_{m4}=g_{m5}$, $C_A=C_1$, and $C_B=C_2=C_3$, a transfer function of a 2nd-order band-pass filter in Eq. (2) is realized.

$$T(s) = \frac{-s\dfrac{g_{mA}}{C_1}}{s^2 + s\dfrac{g_{mA}}{C_A} + \dfrac{g_{mA}g_{mB}}{C_A C_B}} \qquad (2)$$

Equation (3) shows the general equation of the transfer function of 2nd-order band-pass filters.

$$T(s) = \frac{s\dfrac{\omega_0}{Q}}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2} \qquad (3)$$

Comparing Eq. (2) with Eq. (3), the center angular frequency ω_0 (center frequency f_0) and the quality factor Q of the

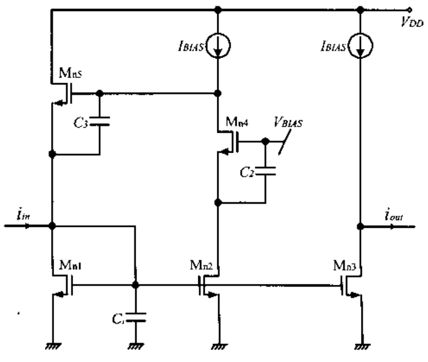


Figure 1. Conventional band-pass filter.

AP-ASIC '02, August 6-8, 2002, Taipei, Taiwan R.O.C.

conventional circuit are shown in Eqs. (4) and (5), respectively.

$$\omega_0 = \sqrt{\frac{g_{mA} g_{mB}}{C_A C_B}} \quad \left(f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{g_{mA} g_{mB}}{C_A C_B}} \right) \tag{4}$$

$$Q = \sqrt{\frac{g_{mB} C_A}{g_{mA} C_B}} \tag{5}$$

It is confirmed from Eqs. (4) and (5) that f_0 and Q can be designed independently by the transconductance values g_{mA} and g_{mB}, and by the capacitance values C_A and C_B. However, Q value mostly tend to be determined by the ratio between C_A and C_B in practical uses. Thus, whole capacitance value become larger as Q value becomes higher. Therefore, it is problem that the whole implementation area of the additional capacitors become larger. This is a obstacle to integration.

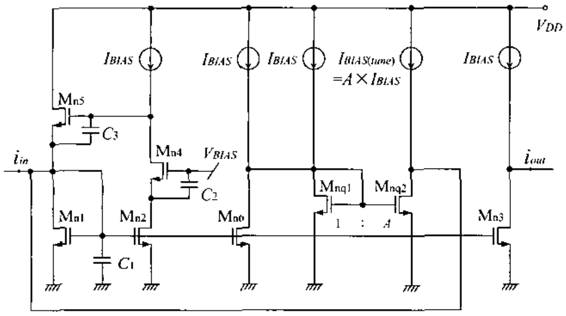
3. PROPOSED CIRCUIT

3.1 Fundamental

Figure 2 shows a figure that explain the principle of the proposed circuit, and Fig. 3 shows the block diagram of the proposed filter. The proposed filter applies Q-enhancement technique [3] to the conventional filter in Fig. 1. Q-enhancement is a technique that can supply high Q by controlling a 1st-order term in the denominator of the transfer function determines Q value by using a positive feedback. Equation 6 shows the transfer function of this proposed circuit.

$$T(s) = \frac{-s\dfrac{g_{mA}}{C_A}}{s^2 + s\dfrac{(1-A)g_{mA}}{C_A} + \dfrac{g_{mA} g_{mB}}{C_A C_B}} \tag{6}$$

Where a variable A in Eq. (6) is the transconductance ratio of M_{nq1} to M_{nq2} ($g_{m(nq1)}$ to $g_{m(nq2)}$), shown as Eq. (7).



Note : “ 1 : A ” in this figure is the ratio between the aspect ratios of M_{nq1} and M_{nq2}

Figure 2. Fundamental of proposed circuit.

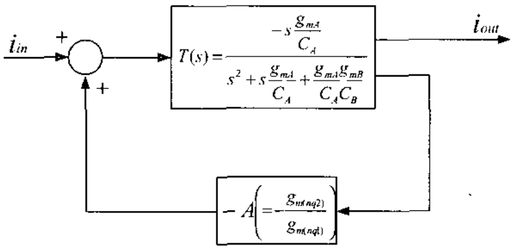


Figure 3. Block diagram of proposed circuit.

$$A = \frac{g_{m(nq2)}}{g_{m(nq1)}} \tag{7}$$

Comparing Eq. (6) with Eq. (3), the center angular frequency ω_0 (the center frequency f_0) and Q of the proposed filter are shown in Eqs. (8) and (9), respectively.

$$\omega_0 = \sqrt{\frac{g_{mA} g_{mB}}{C_A C_B}} \quad \left(f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{mA} g_{mB}}{C_A C_B}} \right) \tag{8}$$

$$Q = \frac{1}{1-A}\sqrt{\frac{g_{mB} C_A}{g_{mA} C_B}} \tag{9}$$

From Eq. (9), it is confirmed that Q value can be designed not only with the ratio of two capacitance values similar to the conventional band-pass filter, but also the variable A. Thus, the capacitance ratio need not to been higher, as Q value becomes higher. Therefore, since a large capacitors are not needed, the proposed filter suites to the integration from the viewpoint of the chip area.

3.2 Design Method of Q Value

In this section, a design method of Q in the proposed circuit is presented. To make this explanation simple, we explained it on assumption that transcouductances of MOSFETs in Fig. 2 (except for M_{nq2}) are the same value, and that capacitance values C_A and C_B are the same value, too (in short $C_A : C_B = 1 : 1$).

First of all, We must settle the appropriated A value for desired Q value. Equation 10 shows the relationship between the A value and the desired Q value.

$$A = \frac{Q-1}{Q} \tag{10}$$

Once the A value has been fixed, the value of the bias current $I_{BIAS(tune)}$ must be settle to the value of A times larger than that of the other bias currents I_{BIAS} as shown in Eq. (11), and the aspect ratio of M_{nq2} must be settle to the value of A times larger than that of M_{nq1} as shown in Eq. (12), too.

$$I_{BIAS(tune)} = A \times I_{BIAS} \tag{11}$$

$$\frac{W_{(nq2)}}{L_{(nq2)}} = A \times \frac{W_{(nq1)}}{L_{(nq1)}} \tag{12}$$

As a result, transconductances of M_{nq1} and M_{nq2} can be settle to have the ratio “$g_{m(nq1)} : g_{m(nq2)} = 1 : A$”, as shown in Eq. (13).

$$g_{m(nq2)} = \sqrt{2\mu_0 C_{ox} \frac{W_{(nq2)}}{L_{(nq2)}} I_{BIAS(tune)}} = A\sqrt{2\mu_0 C_{ox} \frac{W_{(nq1)}}{L_{(nq1)}} I_{BIAS}}$$
$$= A \times g_{m(nq1)} \tag{13}$$

K_0 : Transconductance Parameter.
μ_0 : Carrier Mobility.
C_{ox} : Unit Capacitance of Gate Oxide.
L_i : Channel Length.
W_i : Channel Width.

Where μ_0, C_{ox}, W, and L are used usual meanings. In consequence, the design of desired Q value can be realized.

Figure 4 shows the proposed circuit that we have been simulated. Since the accuracy of Q value depends on the accuracy of the bias current in this circuit, the proposed band-pass filter in this figure is composed using wide swing cascord current mirrors.

3.3 Effects of Area Efficiency of Additional Capacitance

In this section, effects of area efficiency of additional capacitances are presented. Theoretically, the whole capacitance value ratio of the conventional circuit and the proposed circuit needed in design is shown in Eq. (14).

$$\frac{\text{Whole Capacitance Value of Proposed Circuit}}{\text{Whole Capacitance Value of Conventional Circuit}} = \frac{3Q}{Q^2+2} \quad (14)$$

Whole implementation area of the additional capacitor is proportional to whole capacitance value needed in design. An example of the percentage of the area of the proposed circuit per the area of the conventional one for each Q value is shown in Table 1. From this table, it is confirmed that whole area of the additional capacitor needed in design is certainly decreased proportional to under the condition $Q>2$. Therefore, the proposed circuit is expected to suit to integration than the conventional one.

3.4 Implementation

The proposed circuit have been implemented using 1.2μm double-poly, double-metal CMOS process. The micrograph of the prototype chip is shown in Fig. 5. The design value of the filters is that center frequency is 10MHz and Q is 10. Note that in this circuit, two of the three capacitors in Fig. 4 are substituted for parasitic capacitors of two large MOSFETs.

4. SIMULATION RESULTS

The performance of the proposed filter are confirmed by SPICE simulations. In these simulations, MOSIS's 0.5μm technology LEVEL3 model parameters are used. Table 2 shows the simulation conditions and parameters. The design values are set in such a way that the center frequency f_0 is 10 MHz, and Q is 2, 4, 10, and 20.

Figure 6 shows the frequency responses of the current gain of the proposed circuit. It is confirmed that the proposed circuit can certainly realize band-pass characteristics whose center frequencies almost agree with the design value, and also confirmed that the proposed circuit have high current gain near the center frequency.

Figure 7 shows the relationship of the design value and the simulation result. The larger error between the design value and the simulation result occurs when the Q value is increased. It is believed that this error is due to the parasitic capacitors and the resistances that are omitted in the transfer function analysis. Therefore, Q-tuning is needed.

Table 1. Effect of area efficiency with each Q value.

Design value of Q	Area of Additional Capacitors (Proposed / Conventional)
Q=2	100.0 %
Q=4	66.7 %
Q=10	29.4 %
Q=20	15.0 %

Table 2. Simulation conditions.

Name	Value
V_{DD}	3 [V]
V_{BIAS1}	2 [V]
V_{BIAS2}	1.5 [V]
V_{BIAS3}	1 [V]
$V_{(q\text{-}tune)}$	0 [V]
I_{BIAS}	100 [μA]
$I_{BIAS\,(tune)}$	A×100 [μA]
M_{ni} $(i$=1-10), M_{nqi} $(i$=1, 3, 4, 5, 7, 8)	L=1 [μm], W=10 [μm]
M_{nqi} $(i$=2, 6)	L=1 [μm], W=A×10 [μm]
M_{pi} $(i$=1-10), M_{pqi} $(i$=1-4)	L=2 [μm], W=80 [μm]
C_1, C_2, C_3	8.3 [pF]

Figure 8 shows an example of the bulk control Q-tuning when Q is designed at 10 [4]. It is confirmed from this figure that Q value of the proposed filter can be tuned by the voltage between

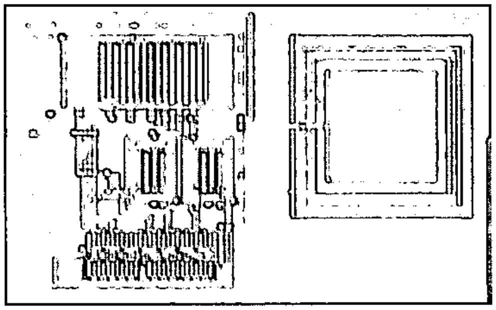


Figure 5. Micrograph of the prototype chip.

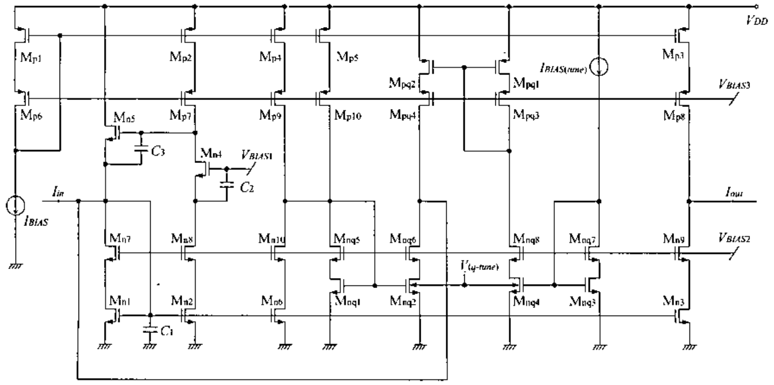


Figure 4. Proposed Band-Pass Filter.

the bulk and source terminal of M_{nq2}, M_{nq4} ($V_{(q\text{-}tune)}$), not changing the center frequency.

Figure 9 shows the relationship between amplitude of peek-to-peek input signal current and total harmonic distortion (THD) at 10MHz. It is confirmed from this figure that the proposed filter in Fig. 4 is high level THD as a whole, specially in case that the amplitude of input signal current is large. Using a fully differential configuration [5], the large THD can be decreased, however the area becomes almost two times.

5. CONCLUSIONS

In this paper, a current-mode area-efficient band-pass filter is proposed. By using Q-enhancement technique, whole capacitance value needed in design can be reduced than the conventional one. Thus, the area of the filter circuit itself can be decrease on an IC chip.

However, this propose circuit have some problems for practical use, for example, a stability by using a positive feedback, a difficulty in higher Q setting, and a narrow dynamic range by high current gain in passband and so on.

6. ACKNOWLEDGMENTS

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by On-Semiconductor, Nippon Motorola LTD., HOYA Corporation, and KYOCERA Corporation.

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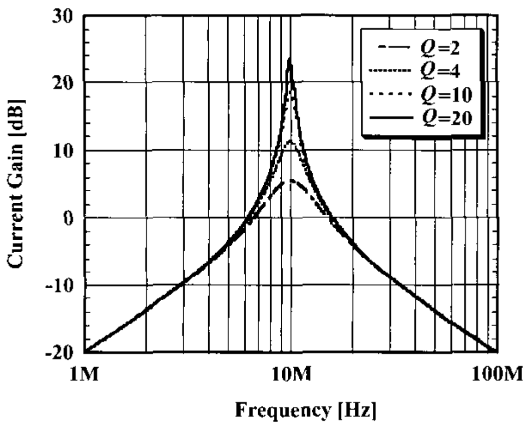

Figure 6. Frequency responces of current gain.

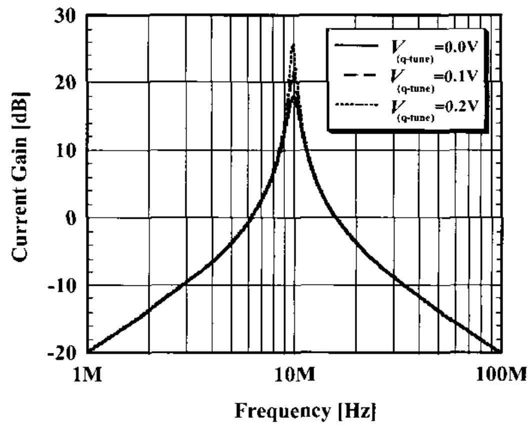

Figure 8. Example of bulk-controlled Q-tuning (Q=10).

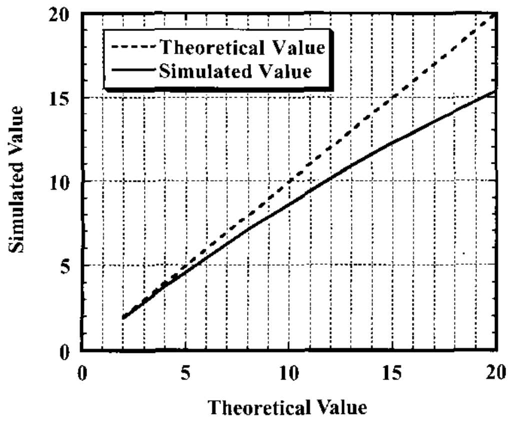

Figure 7. Comparison of design value and simulation result of Q

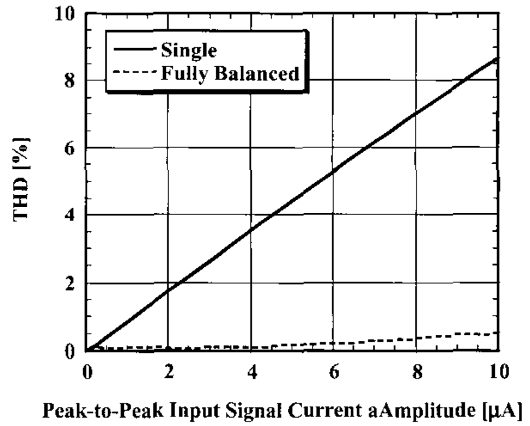

Figure 9. Relationship between amplitude of peak-to-peak input signal current and THD.